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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,587	01/28/2004	Miwa Wake	S004-4839 (DIV)	3839

7590 09/19/2005

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EXAMINER	
TRAN, THANH Y	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,587	WAKE ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 2-5 is/are allowed.

6)☒ Claim(s) 6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art that is submitted by Applicant (figures 7A-7F) in view of Shukuri et al (U.S. 6,541,333).

As to claim 6, figures 7A-7F of the admitted prior art discloses a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film (7) provided on a first conductivity type supporting substrate (3) through an embedded insulating film (2), comprising: a second conductivity type source region (141) and a second conductivity type drain region (151) formed in the semiconductor film (7); a gate insulating film (13) formed on an upper surface of the semiconductor film (7); and a gate electrode (12) formed on an upper surface of the gate insulating film (13), wherein a channel region (source/drain region) situated under the gate insulating film (13) has a first conductivity type impurity region (a first conductivity type impurity region can be a region between the source and the drain regions).

The admitted prior art (figures 7A-7F) does not disclose a first conductivity type impurity region having a higher density than a well at a boundary with the drain region.

Shukuri et al discloses in figure 68(a) a semiconductor integrated circuit comprising: a first conductivity type impurity region (15b) having a higher density than a well at a boundary

with the drain region (15a) (see col. 13, lines 50-64). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor integrated circuit of the admitted prior art (figures 7A-7F) by having a first conductivity type impurity region having a higher density than a well at a boundary with the drain region as taught by Shukuri et al for forming a lightly doped drain structure.

Allowable Subject Matter

3. Claims 2-5 are allowed.

4. The following is a statement of reasons for the indication of allowable subject matter:

Claim 2 recites, inter alia, "*a method of manufacturing a semiconductor integrated circuit, in which a CMOS transistor is formed on a first conductivity type semiconductor film provided on a first conductivity type supporting substrate through an embedded insulating film, comprising the steps of: conducting thermal oxidation to form a LOCOS for element separation between transistors in the semiconductor film; forming a second conductivity type impurity region in an ultra-shallow portion of each of a source region and a drain region; forming a second conductivity type impurity region having a low density in a middle portion of each of the source region and the drain region; forming a second conductivity type impurity region having the same density as the second conductivity type impurity region in the ultra-shallow portion in a lower portion of each of the source region and the drain region*"; and in the combination with other claimed limitations.

Claim 3 recites, inter alia, "*a method of manufacturing a semiconductor integrated circuit, in which a CMOS transistor is formed on a first conductivity type semiconductor film provided on a first conductivity type supporting substrate through an embedded insulating film,*

comprising the steps of: conducting thermal oxidation to form a LOCOS for element separation between transistors in the semiconductor film; forming a first conductivity type impurity region having a higher density than that of the first conductivity type impurity region in a middle depth portion of the semiconductor film serving as the proximal region to a drain in the first conductivity type impurity region; and performing ion implantation through the gate electrode so as to form a second conductivity type impurity region in each of a source region and a drain region"; and in the combination with other claimed limitations.

Claim 4 recites, inter alia, "*a semiconductor integrated circuit, in which a CMOS transistor is formed on a first conductivity type semiconductor film provided on a first conductivity type supporting substrate through an embedded insulating film, comprising: a source region includes an ultra-shallow high-density N-type source region at a boundary with a channel region, a low-density N-type source region under the ultra-shallow high-density N-type source region, and an embedded insulating neighboring N-type source region; and a drain region includes an ultra-shallow high-density N-type drain region at a boundary with the channel region, a low-density N-type drain region under the ultra-shallow high-density N-type drain region and an embedded insulating neighboring N-type drain region*"; and in the combination with other claimed limitations.

The prior art of record does not teach or render obvious to modify the art of record so as to include the above mentioned-limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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